Characteristics of Trenched Coplanar Waveguide for High-Resistivity Si MMIC Applications

Suidong Yang, Zhirun Hu, Neil B. Buchanan, Vincent F. Fusco, *Senior Member, IEEE,* J. A. Carson Stewart, *Member, IEEE,* Yunhong Wu, B. Mervyn Armstrong, *Member, IEEE,* G. A. Armstrong, and Harold S. Gamble, *Member, IEEE*

***Abstract*— A novel low RF loss trenched coplanar waveguide (CPW) transmission-line structure fabricated using evaporated aluminum tracks on a high-resistivity (10-k$\Omega\cdot$ cm) silicon (HRS) substrate is reported. By assuming that Schottky contact boundaries exist at the metal silicon substrate interface in the CPW line, the finite-element analysis method is used to determine the simulated behavior of the structure. The distributed capacitance, leakage conduction current, and dynamic shunt conductance for the line are shown to be a function of dc bias applied to the line, and also to reduce as a function of trench depth in the normal bias regime. Experimental results show: 1) the reduction of RF losses in comparison with conventional aluminum conductor CPW line structures may be as much as 0.5 dB/cm at 30 GHz; 2) by proper positive dc biasing of a CPW line on a p-type HRS substrate, a further reduction (0.2 dB/cm) in RF loss at 30 GHz can be achieved; 3) predicted trends in line leakage current, capacitance, and relative characteristics impedance are experimentally verified. The proposed waveguide structure may be utilized in a special fabrication process designed for RF/microwave applications.**

***Index Terms*—Capacitance, conductance, CPW, loss, MMIC.**

I. Introduction

MILLIMETER-WAVE frequencies are being proposed for high-volume low-cost/size/mass commercial applications. These applications include sensors for vehicle monitoring and control, radio local area networks (LAN's), secure cellular-radio systems, and short-range wide-band radio links. To achieve low cost with moderate-to-high-volume circuit production, monolithic circuitry is preferred. At microwave frequencies monolithic microwave integrated circuits (MMIC's) employ GaAs technology with integrated active devices. However, GaAs real estate is expensive, particularly when passive circuit elements occupying large areas are required, e.g., filters, diplexers, antennas, etc.

A number of alternative substrates can be considered for planar millimeter-wave circuit or interconnect design. While GaAs offers low dielectric loss, high dielectric constant, and compatibility with MESFET and high electron-mobility transistor (HEMT) active-device technology, it is recognized that large-area GaAs substrates are costly to produce with low defect density. Silicon technology is mature, both for the production of uniformly polished high purity substrates, and for device fabrication and integration. High-resistivity silicon (HRS) offers constant thickness and high dielectric constant which is stable with frequency. In addition, polished silicon wafer substrates are very cost effective, and it has been reported that transmission lines on silicon substrate material have acceptable RF losses even in the microwave-frequency regime [1]–[4].

By employing silicon as a low-cost low-loss substrate medium, relatively large-area passive elements can be realized at millimeter-wave frequencies. Moreover, discrete silicon or GaAs devices [5] can be incorporated into these silicon circuits. This provides a flexible technology for planar circuits in which the active device most suitable for a particular task may be employed. A future extension may be the direct integration of SiGe heterojunction bipolar transistor (HBT) devices to give silicon-based circuits the capability of efficient operation at high microwave frequencies [6], [7]. The HRS substrate has been reassessed as a potential microwave material for MMIC's by Reyes *et al.* in 1995 [4] and, most recently, by Burghartz *et al.* [7]. Reyes *et al.* show that the RF dissipation loss in a coplanar waveguide (CPW) line constructed directly on an HRS substrate is one order lower than that of a CPW line with an oxide insulation layer between metal and semiconductor. In this paper, we demonstrate that a reduction in RF dissipation loss can be realized by means of trenching the HRS substrate and by dc biasing the CPW signal line. The proposed waveguide structure may be utilized in a special fabrication process designed for RF/microwave applications.

At the signal frequencies lower than 100 GHz, the transmission losses in conventional CPW lines are mainly contributed by conductor ohmic loss and dissipation loss within the dielectric substrate material. Conductor loss is influenced by

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S. Yang, N. B. Buchanan, V. F. Fusco, and J. A. C. Stewart are with the High-Frequency Electronics Laboratory, Department of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast, BT9 5AH, Northern Ireland.

Z. Hu was with the High-Frequency Electronics Laboratory, Department of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast, BT9 5AH, Northern Ireland. He is now with GEC Marconi Instruments, Stevenage, Herts., SG1 2BA, U.K.

Y. Wu, B. M. Armstrong, G. A. Armstrong, and H. S. Gamble are with the Northern Ireland Semiconductor Research Centre, Department of Electrical and Electronic Engineering, The Queen's University of Belfast, Belfast, BT9 5AH, Northern Ireland.

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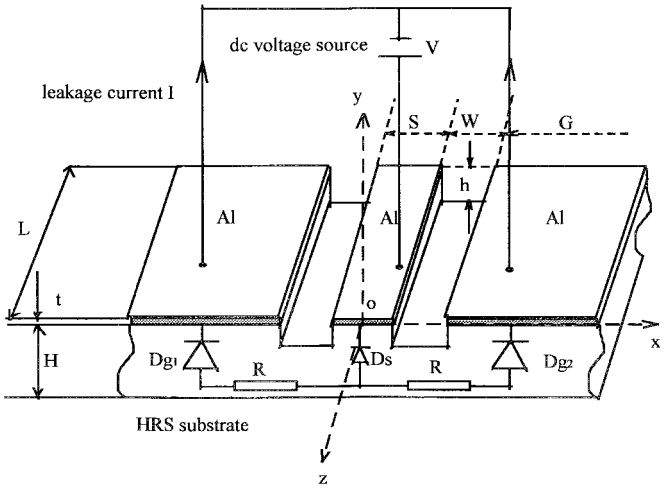


Fig. 1. Schematic diagram of the modeled trenched CPW line and its electrical equivalent circuit.

the conductivity of the metal, and the conduction current distributions on the CPW lines. Substrate dissipation loss is dependent on the leakage conduction current distribution and the electric-field distribution in the semiconductor substrate. The metal–semiconductor contacts between CPW metallization and the host silicon substrate in conjunction with different designed line configurations will lead to a variety of electric-field patterns. These, in turn, result in different conduction current distributions, different line shunt conductances, and ultimately, different RF losses.

In this paper, we illustrate the effect on electric-field, conduction current, distributed capacitance, and characteristic impedance due to vertically etched side grooves in the gaps in the CPW line between signal and ground tracks, as shown in Fig. 1. Each of these is evaluated as a function of the dc bias on the CPW signal track with respect to its ground planes. A number of theoretical predictions are presented and compared with experimental results. The effects of temperature on transmission lines based on silicon substrate have been previously reported in [7] and [8].

II. A Physically Based Device Model for Trenched CPW Lines

The typical electromagnetic field distributions obtained for a conventional dielectric substrate-based CPW line by Gupta in 1981 [9] are altered by the presence of trench effects and metal–semiconductor contact effects. Consider a trenched CPW line based on HRS substrate, as shown in Fig. 1. This is constructed on (H) 650-μm-thick 10-k$\Omega\cdot$ cm p-type silicon substrate with $\langle 100 \rangle$ crystal orientation. The line dimensions are selected to give an approximate 50-Ω characteristic impedance on an untrenched line and simultaneously to accommodate 200-pitch ground–signal–ground (GSG) CPW probes. Line spacing W is 40 μm, signal track width S is 70 μm, and line length L is 6100 μm. The widths of the ground lines G are 2.5 mm. Using standard silicon-processing methods, a 1.46-μm-thick (t) aluminum metallization layer is evaporated onto the HRS substrate (this is thinner than the thickness of 4 μm associated with three skindepth penetration on bulk aluminum for a nominal operating frequency of 30 GHz).

For most semiconductors (owing to the presence of interface states), when metal is evaporated directly onto the HRS, a metal–semiconductor Schottky barrier is formed [10]. The actual barrier height is determined by the property of the semiconductor surface and the contact metal. Schottky contacts in the simulation are modeled by the work function of the electrode metal and an optional surface recombination velocity (in this paper, values of 4.71 eV and 1.62 $\times$ 10^6 m/s are used, respectively). The CPW trench depths (h) examined are 0, 3, 6, 9, and 12 μm. Trenching is obtained by processing the substrate in a capacitively coupled glow–discharge plasma excited by a 70-W 13.56-MHz RF source at CF_4 pressure of 150 mtorr. The observed silicon etch rate is about 1.5 μm per hour. The silicon surface charges are assumed negligible in the trench. Based on the nominal resistivity, the p-doping density is around the order of 10^{12} cm^{-3}.

For the geometry in Fig. 1 the two-dimensional Poisson's equation, electric-charge carrier motion equations, and carrier continuity equations in the CPW line based on the HRS substrate are solved selfconsistently by the finite-element-analysis method using a commercial semiconductor device simulation package.[1] Results from the simulation are as follows.

1) Typical static electric-field line distributions in the trenched CPW lines are shown in Fig. 2 for different trench depths. From these, it can be seen that there are some special regions near the silicon surface where the electric line distributions are radically different from those of the classical CPW case. It is also interesting to note that the depth of this region is of the order of the silicon diode depletion region depth (10–20 μm), which has been estimated for an applied reverse bias voltage 2.0 V and a p-silicon doping concentration 1–3 $\times$ 10^{12} cm^{-3}, bulk resistivity 10 k$\Omega\cdot$ cm [11]. Furthermore, as can be seen, the maximum electric fields are effectively decreased as the trenched depth increases. In each case, the dc-voltage difference between signal line and ground plate is chosen to be 2.0 V.
2) The corresponding leakage conduction–current contour distributions are shown in Fig. 3. As can be seen, the current density with its pattern crowding at the edges of the signal and ground lines is effectively reduced as the trenching depth increases.
3) Simulated distributed capacitance versus signal bias is plotted for different trenched CPW lines in Fig. 4. All of the distributed capacitances show a nonlinear response as the signal bias changes, owing to the presence of two metal–semiconductor contact layers which act as two back-to-back Schottky diodes, as shown in Fig. 1. The trend that a maximum capacitance is formed

[1] *SILVACO Int. ATLAS User's Manual, Device Simulation Software, Edition 4*, Oct. 30, 1996, pp. 3-2–3-54.

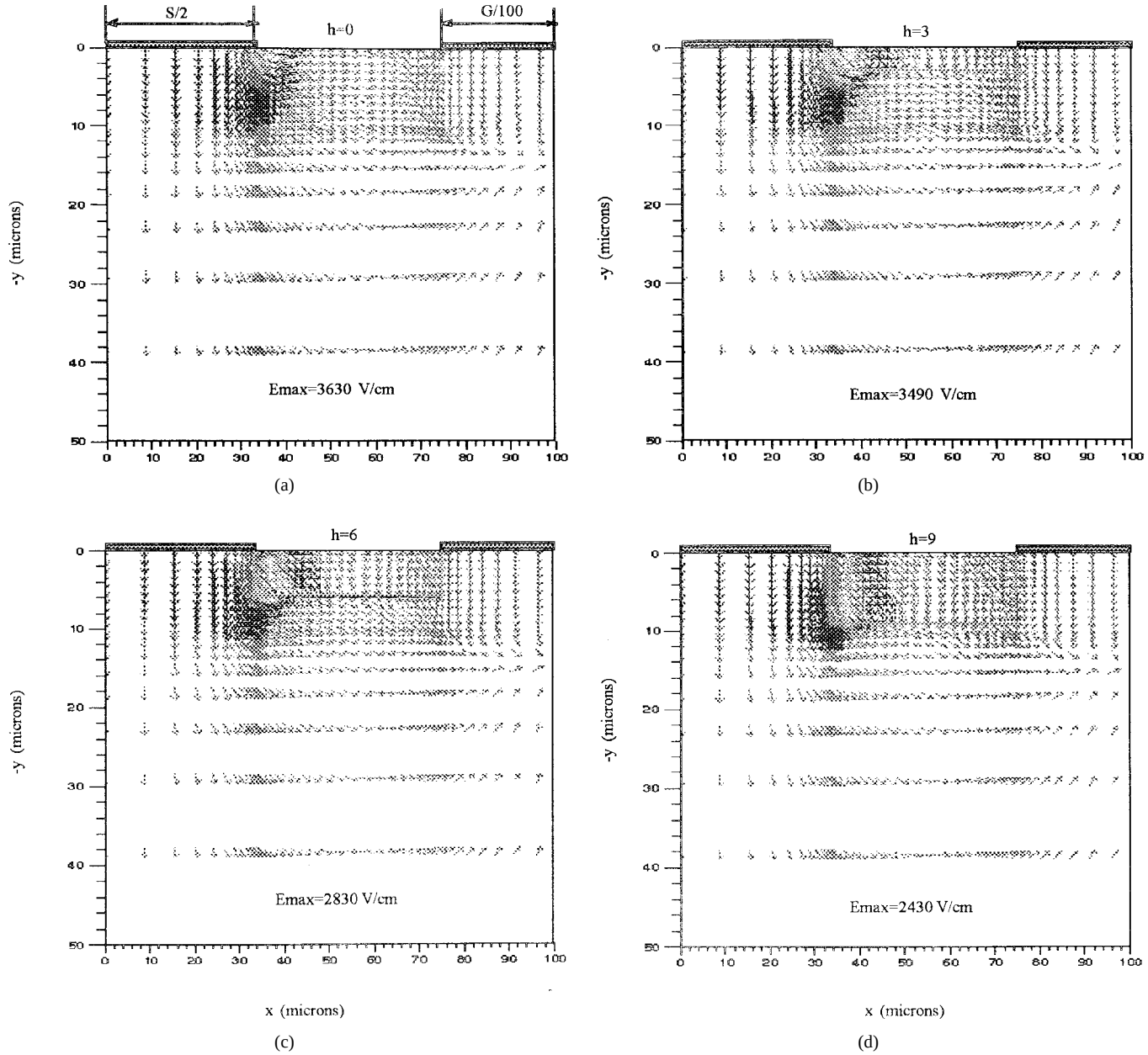


Fig. 2. *E*-line distributions in modeled CPW devices.

around zero-bias operation occurs, since at least one of the Schottky diodes is always in the reverse operation regime when the signal bias is moved away from the zero-bias point. Moreover, the asymmetry of CV curves with increased bias can be eliminated in the simulation by equating the ground track width G to one half of the signal linewidth.

4) Simulated dynamic shunt conductance versus signal bias for different trenched CPW lines is shown in Fig. 5. For negatively bias (forward) operation, the dynamic shunt conductance of the modeled CPW line is relatively larger than that of positively biased (reverse) case. This is due to the difference of two Schottky diodes. In the zero bias and reverse bias regimes, relatively small leakage currents are induced; here, the calculated shunt conductance is reduced as the trench depth increases. However, for large forward bias (GSG voltage < -3.0 V), large leakage currents are induced. Simulated results show that unlike the reduced CPW line capacitance which occurs with increased trench depth, the deeper the trench, the larger the shunt conductance.
5) The simulated total distributed capacitance C_t, the total leakage current I_t (electron plus hole motion current), the effective shunt conductance G_d, and the normalized characteristic impedance as function of trench depth h are listed in Table I.
6) Simulated leakage current versus signal bias for different trenched CPW lines is shown in Fig. 6. As can been seen, the *I–V* curve at different trench depth shows the forward and reverse current–voltage characteristics of a

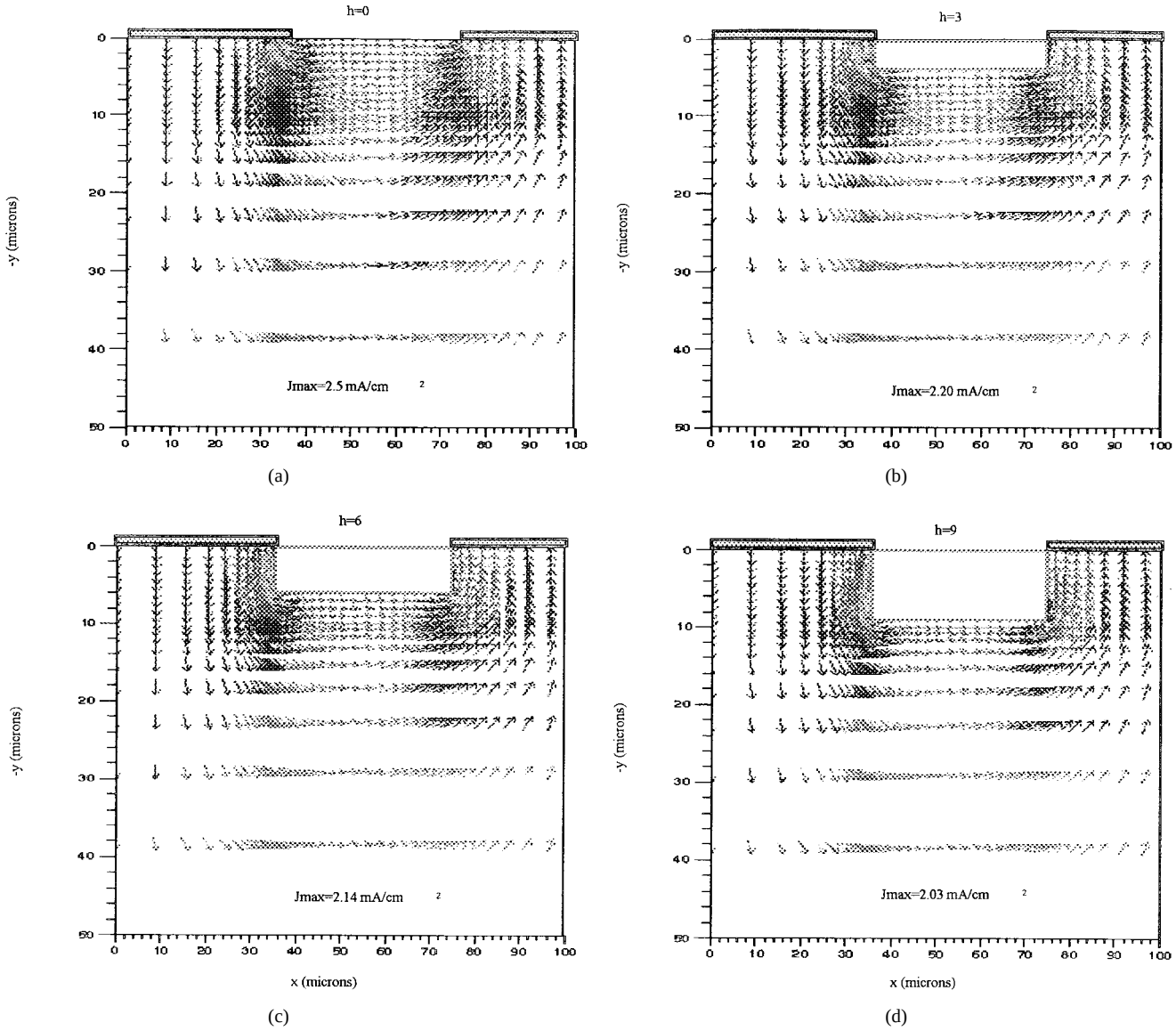


Fig. 3. Current flow patterns in modeled CPW devices.

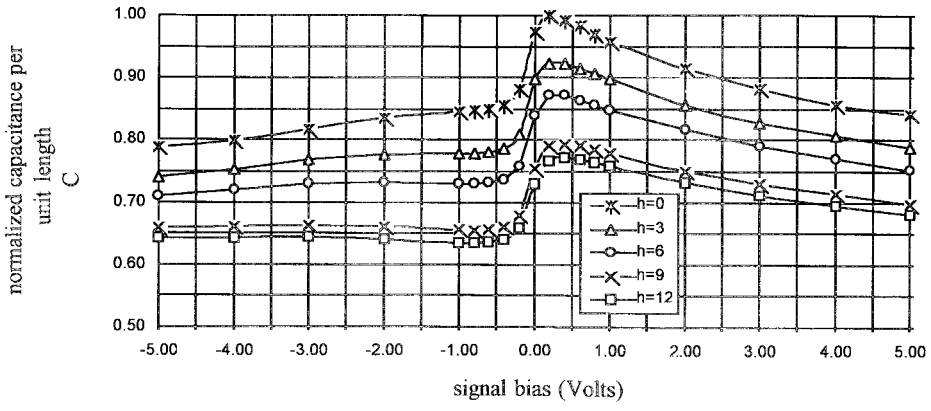


Fig. 4. Simulated distributed capacitance per unit length in trenched CPW lines as function of signal bias.

back-to-back diode pair. Both the currents for positive and negative bias are reduced due to the trenching effects.

In Table I, the electrostatic distributed capacitances are estimated using the derivative of the induced electrical charge on the signal line with respect to variation of signal voltage, i.e., a small ac analysis approach [12]. For a nontrenched CPW line, the calculated capacitance per unit length (1.42 pF/cm) is 18% smaller than the 1.7 pF/cm (that of a conventional CPW line with an ideal dielectric constant), estimated by conformal

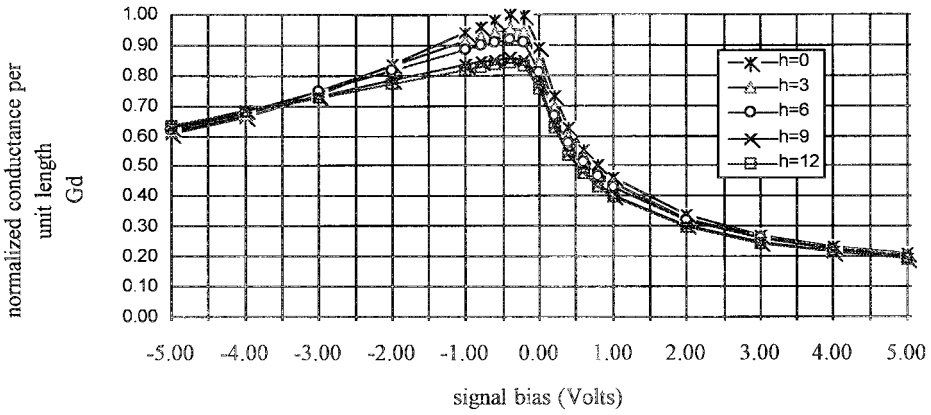


Fig. 5. Simulated shunt conductance per unit length as function of signal bias.

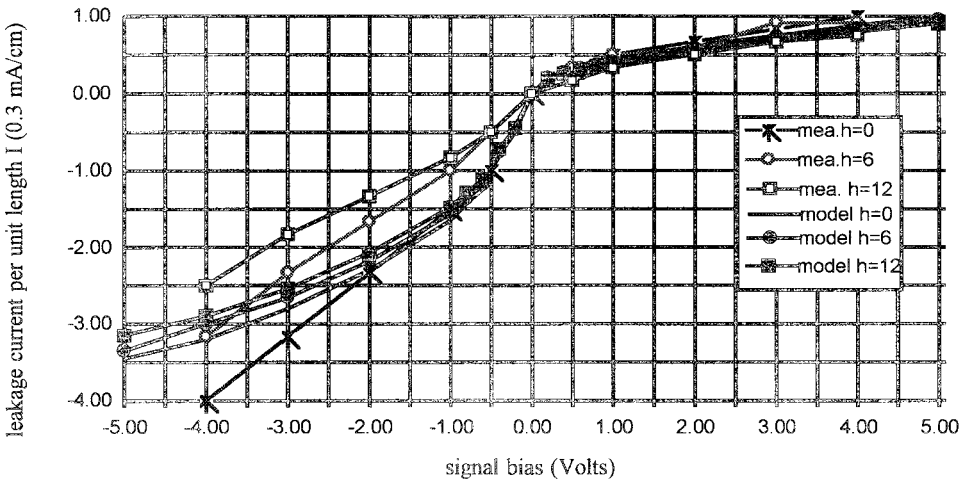


Fig. 6. Simulated and measured *I–V* curves for different trenched CPW lines.

TABLE I
SIMULATED PARAMETERS. HERE, GSG VOLTAGE = 2.0 V, $Z_0 = 53.8\ \Omega$ BASED IN QUASI-STATIC ANALYSIS [8], [11]

Trench depth h (μm)	0	3	6	9	12
Ct (PF/cm)	1.42	1.26	1.18	1.10	1.04
It (μA/cm)	167	162	157	150	137
Gd ($10^{-5}\Omega^{-1}$/cm)	6.67	6.46	6.33	6.02	5.92
Z_c/Z_0	1	1.06	1.10	1.14	1.17

mapping techniques [9], [13]. The total leakage conduction current is obtained from the surface integral of the modeled current flow distribution. The dynamic shunt conductance is evaluated from the derivative of signal voltage with respect to the induced variation of leakage current. Finally, the normalized characteristic impedance for different trenched CPW lines is estimated by the formula $Z_h/Z_0 = \sqrt{C_0/C_h}$, where Z_0, C_0 refer to the characteristic impedance and capacitance for the nontrenched CPW line with the effective dielectric constant $\varepsilon_r = 1$. As this equation comes from a quasi-static consideration [9] and uses the static capacitance, it is a lossless line estimation and, therefore, only an approximation. As can be seen from Table I, the distributed capacitance, leakage conduction current, and shunt conductance have been shown to be reduced, owing to the trench effects. The characteristic impedance increases by a factor of 1.17 as the trench depth increases from 0 to 12 μm.

III. MEASUREMENT

I–V measurements of CPW lines fabricated according to the previous specifications were carried out by use of an HP 41424A modular dc source/monitor and cascade wafer probe station (typical curves being shown in Fig. 6). The leakage currents are reduced as the trench depth increased, and the measured reverse saturation currents are comparable with the simulated results. These nonlinear characteristics can be explained by the existence of two back-to-back diodes below the signal and ground plate, as shown in Fig. 1. Here, the leakage current path is completed through Schottky diodes $D_{g1,2}$, D_s, and bulk silicon resistor R. It should be remembered that although the area of the $D_{g1,2}$ Schottky diode is much greater than the D_s center diode, the nonlinear leakage current in the electric path is mainly influenced by the reverse biased diode.

CV curves for the CPW line were obtained by use of a wafer probe station and an HP 4275A multifrequency inductance, capacitance, and resistance (ICR) meter at an RF (10-MHz) amplitude of 0.01 V (peak-to-peak). The results (shown in Fig. 7) show the same basic trend as the simulations in Fig. 4.

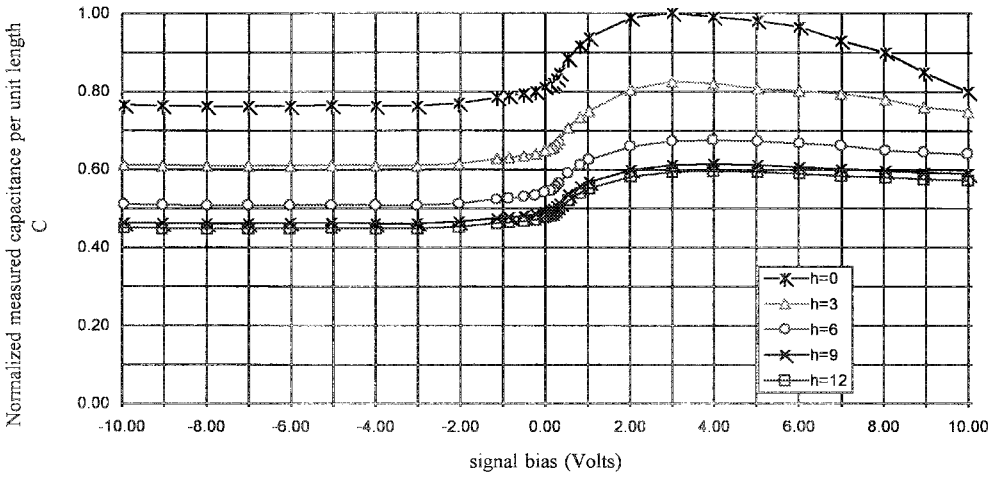


Fig. 7. Measured CV curves in different trenched CPW lines.

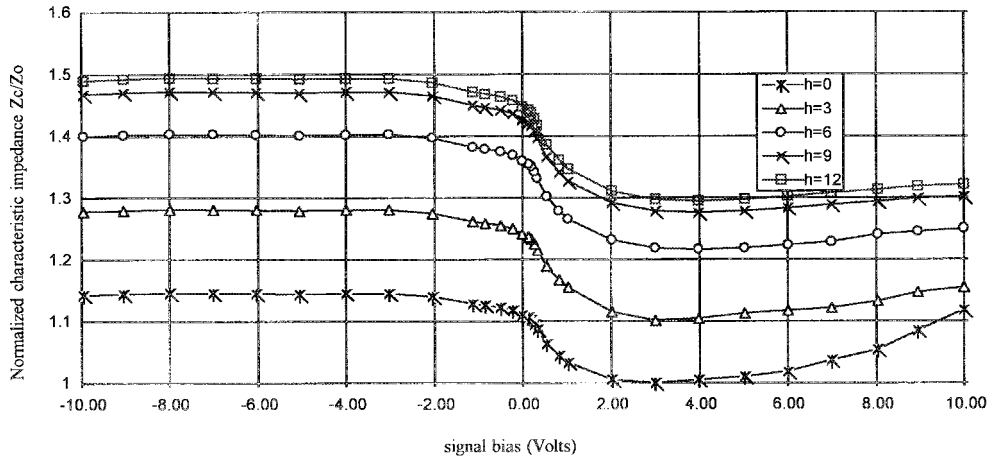


Fig. 8. Characteristic impedance extracted from measured CV data for different trenched CPW lines.

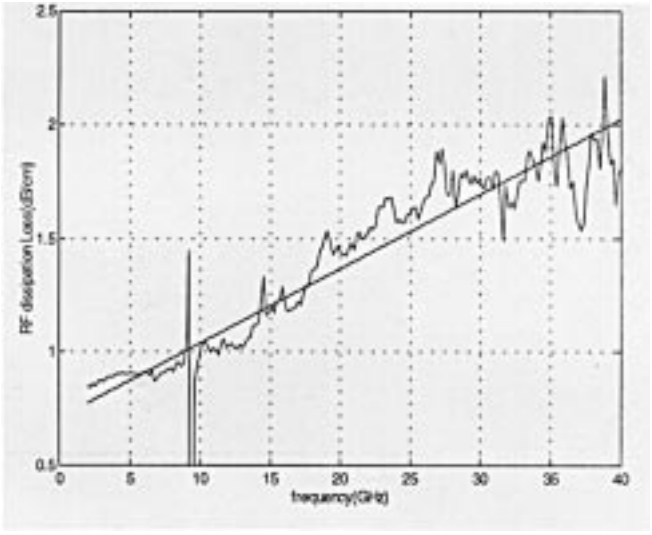
TABLE II
MEASURED RF PARAMETERS VERSUS SIGNAL BIAS FOR A CPW LINE ($h = 0$) BASED ON HRS ($\rho = 10$ kΩcm) SILICON 4-in WAFER AT SPOT FREQUENCY OF 30 GHz

GSG (Volts)	0.0	1.0	2.0	3.0	4.0
$\lvert S_{11}\rvert$	0.1036	0.1036	0.1033	0.1036	0.1033
$\lvert S_{21}\rvert$	0.8682	0.8783	0.8811	0.8818	0.8826
RF loss (dB/cm)	1.94	1.77	1.73	1.71	1.70
$\lvert Z_c\rvert$ (Ohms)	49.0	49.0	49.1	49.2	49.2

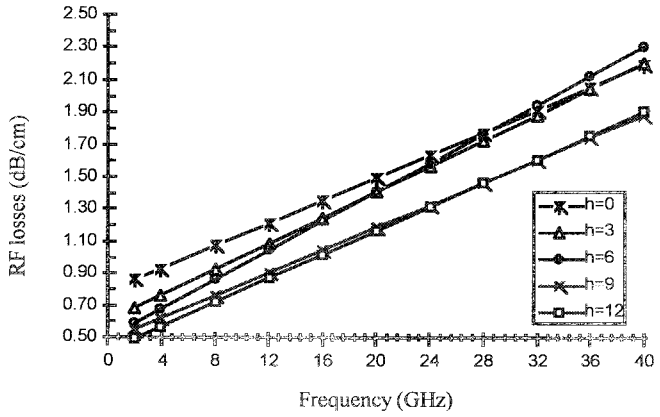
However, the peaks on curves in Fig. 7 are shifted to the forward bias direction compared with those in Fig. 4. This phenomena is under further examination. Fig. 8 shows the corresponding characteristic impedance evaluated from the measured capacitances. It can be seen from Figs. 7 and 8 that the equivalent capacitance presented to the propagating wave tends to decrease after the lines are trenched, and the characteristic impedance for 12-μm trenched CPW lines increases roughly by a factor of 1.3 compared to that of nontrenched lines.

Two-port scattering parameters were measured using an HP 8510B network analyzer and cascade wafer probe station with 200-μm GSG coplanar probes calibrated using line–reflect–match (LRM) to the probe tips, taking care to eliminate multireflection losses [14].[2] From the measured scattering parameters of the RF dissipation losses, characteristic impedances of the lines have been evaluated. Typical calculated data are shown in Fig. 9(a)–(c). As can be seen in Fig. 9, without trenches, RF losses are 1.2 dB/cm at 10

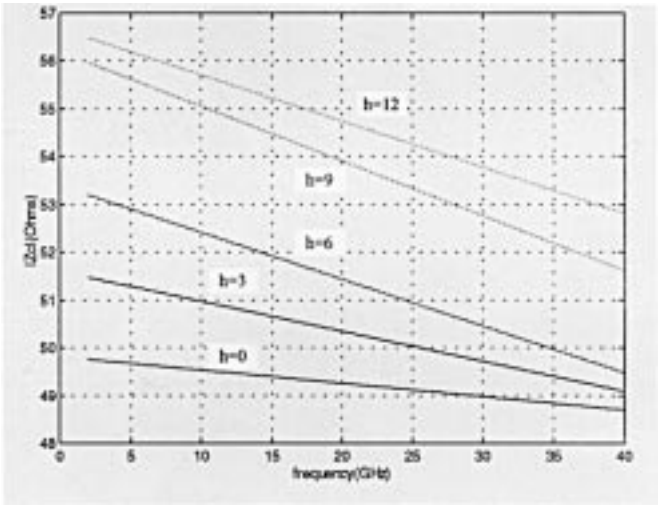
[2] *The RF Capacitor Handbook, American Technical Ceramics*, 1979.



(a)



(b)



(c)

Fig. 9. (a) Typical calculated and linear fitted RF dissipation losses for a trenched CPW line ($h = 3$ μm). (b) Linear fitted RF losses for the trenched CPW lines. (c) Calculated characteristic impedances from measured S-parameters for the trenched CPW lines.

GHz and 1.9 dB/cm at 30 GHz. With 9-μm-deep trenches, the line dissipation losses are reduced to 0.8 dB/cm at 10 GHz and 1.6 dB/cm at 30 GHz. Finally, Table II shows the typical RF losses at different signal bias for a spot frequency of 30 GHz. As can be seen, the losses for zero-bias condition is about 0.2–0.3 dB/cm higher than that for the 4.0-V bias level.

The reduction of RF losses as the signal bias increases may be quantitatively explained by consideration of Fig. 5, in which all of the dynamic shunt conductances in the different trenched CPW lines reduce as the signal bias is increased in the positive direction.

IV. Conclusions

For the first time, the characteristics of trenched CPW's for Si MMIC application have been established both experimentally and by semiconductor device simulation. By introducing a vertical trench in the gaps between signal and ground plate, and by dc biasing the CPW line, RF losses can be reduced. This reduction is primarily due to the smaller substrate leakage conduction current and to the reduction in conductor loss owing to the removal of field concentration from the vicinity of the conductor edges. The proposed waveguide structure may be utilized in a special process designed for RF/microwave applications.

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Suidong Yang was born in Chengdu, Sichuan, China, in 1964. He received the B.S. degree in applied physics from the National Defence University of Science and Technology, Changsa, Hunan, China, in 1984, the M.Phil degree in laser technique from the South-West Institution of Technical Physics, Chengdu, China, in 1987, and the Ph.D. degree from the Open University, Milton Keynes, U.K., in 1998.

From 1987 to 1991, he studied RF excited CW phase-locked CO_2 laser arrays and TEA-pulsed CO_2 lasers in the South-West Institution of Technical Physics, where he was a Research Engineer. From 1993 to 1997, he worked in the Oxford Research Unit, Open University, in the field of low-temperature low-pressure inductively coupled RF plasma in the application of semiconductor processing. In May 1997, he joined the High-Frequency Electronics Research Group, Queen's University of Belfast, Northern Ireland. His current research interests include simulation and diagnostics of RF plasmas, electromagnetic-field theory, microwave detector for silicon MMIC applications, waveguide transmission-line discontinuity modeling, and on-wafer millimeter-wave and semiconductor device-characterization measurement techniques.

Zhirun Hu received the B.Eng. degree in telecommunication engineering from Nanjing Institute of Posts and Telecommunications, Nanjing, China, in 1982, and the Masters degree in business administration and the Ph.D. degree in electrical and electronic engineering from The Queen's University of Belfast, Belfast, Northern Ireland, in 1988 and 1991, respectively.

In 1991, he joined the Electrical and Electronic Department, University College of Swansea, as a Senior Research Assistant in semiconductor device simulation. In 1994, he rejoined the Electrical and Electronic Department, Queen's University of Belfast, as a Research Fellow in silicon MMIC design. In 1996, he joined GEC Marconi Instruments, where he is currently a Microwave Technologist, working on new-generation microwave power sensors. His research interests include computer-aided design and optimization of microwave and millimeter-wave circuits, and semiconductor device simulation and optimization.

Neil B. Buchanan was born in Belfast, Northern Ireland, on May 19, 1972. He received the B.Eng. (Hons) degree from The Queens University of Belfast, Belfast, Northern Ireland, in 1993, and is currently working toward the Ph.D. degree in phase-locked millimeter-wave HEMT oscillators.

Since 1997, he has worked as a Senior Engineer in the High-Frequency Electronics Group, The Queens University of Belfast, where he is involved in several state-of-the-art research activities including millimeter-wave MMIC design and millimeter-wave silicon projects. He also maintains the microwave measurement system and CAD system within the High-Frequency Electronics Group.

Vincent F. Fusco (S'82–M'82–SM'96) received the B.Sc. and Ph.D. degrees from The Queen's University of Belfast, Belfast, Northern Ireland, in 1979 and 1982, respectively.

He has worked as a Research Engineer on short-range radar and radio telemetry systems and is currently Professor of high-frequency electronic engineering in the School of Electrical Engineering and Computer Science, The Queen's University of Belfast, where he is also Head of the High-Frequency Research Group. His current research interests include nonlinear microwave-circuit design, active antenna design, and concurrent techniques for electromagnetic field problems. He has published 150 research papers in these areas and authored *Microwave Circuit, Analysis and Computer Aided Design* (Englewood Cliffs, NJ: Prentice-Hall, 1987). In addition, he is involved with a number of professional committees and has acted as consultant to government, local, national, and international companies.

Prof. Fusco was awarded the NI Engineering Federation Trophy in 1986.

J. A. Carson Stewart (M'88) received the B.Sc. degree in physics and the Ph.D. degree from The Queen's University of Belfast, Belfast, Northern Ireland, in 1959 and 1962, respectively.

After working in Shorts, Belfast, Northern Ireland, as a Design Engineer, he was a Post-Doctoral Fellow at Queen's University, Kingston, Ont., Canada. He is presently Head of the Department of Electrical and Electronics Engineering, Queen's University of Belfast, where he is also Professor of electrical communications. He has published extensively in the areas of CAD and simulation of microwave active devices.

Prof. Stewart is a member of the organizing committee of the UK/ROL IEEE Joint Chapter in MTT/ED/AP/LEO and was Chairman of the 1996 IEEE Microwaves Conference.

Yunhong Wu graduated from Beijing Institute of Technology, Beijing, China, in 1963.

In 1963, he joined Hebei Semiconductor Research Institute, China, as a Research Engineer, where he worked on semiconductor devices, design, and process development. From 1963 to 1968, he developed the Si microwave mixer diode, Si voltage reference diode, Si voltage variable capacitor, Si varactor, and high-power microwave Si p-i-n diode. In 1968, he moved to Nanjing Electronic Devices Institute as a Senior Research Engineer and Head of the Research Group. From 1968 to 1978, he set up an Si microwave p-i-n diodes fabrication pilot line, and developed an Si p-i-n diode for microwave attenuators. From 1979 to 1989, he did research on GaAs microwave power MESFET's, GaAs power MMIC's, and submicron semiconductor process. Since January 1990, he has been with the Northern Ireland Semiconductor Research Centre, The Queen's University of Belfast, Belfast, Northern Ireland, as a Research Fellow, where he developed a large-area ion-shower implanter and process technology for poly-Si thin-film transistors fabrication, and a reative-ion etch (RIE) deep-trench process. His current research areas include Si-MMIC's, superhigh-speed interconnections, fast etch-rate RIE, and SOI techniques.

Mr. Wu is a member of the Electronics Society of China. He received Chinese Science and Technology Awards in 1978 and 1987, and Chinese Outstanding Electronic Technology Awards in 1979, 1982, and 1984.

B. Mervyn Armstrong (M'80) received the B.Sc. and Ph.D. degrees in electrical and electronic engineering from The Queen's University of Belfast, Belfast, Northern Ireland, in 1970 and 1973, respectively.

He is currently a Reader in microelectronics in the Department of Electrical and Electronic Engineering, The Queen's University of Belfast, and Assistant Director of the Northern Ireland Semiconductor Research Centre. He has co-authored over 100 papers. His current research interests include novel technology for SOI applications in high-frequency and ultra-low-power silicon integrated circuits, smart power technology, advanced chemical-vapor deposition technology, and silicon technology for millimeter-wave applications.

Dr. Armstrong is a member of the Institute of Physics, London, U.K.

G. A. Armstrong received the B.Sc. degree in electrical and electronic engineering and the Ph.D. degree from The Queen's University of Belfast, Belfast, Northern Ireland, in 1968 and 1971, respectively.

He spent a number of years working in industry on the development of surface acoustic-wave devices before rejoining the Electrical and Electronic Engineering Department, The Queen's University of Belfast, as a Lecturer, and was appointed Reader in 1990. He currently leads the Semiconductor Device Simulation Research Group, Northern Ireland Semiconductor Research Center. He has acted as a Consultant to four major U.K. semiconductor companies. His current research interests cover all aspects of semiconductor process, device, and circuit simulation, with particular emphasis on silicon on insulator devices, HBT's, and polysilicon thin-film transistors. He has co-authored over 80 research papers and conference publications. He has written several software packages for semiconductor device simulation, which have been utilized by U.K. industry.

Harold S. Gamble (M'95) received the first-class honors degree in electrical and electronic engineering and the Ph.D. degree from The Queen's University of Belfast, Belfast, Northern Ireland, in 1966 and 1969, respectively.

In 1973, he returned to The Queen's University, following a period as a Research Engineer at the Standard Telecommunication Laboratories, Harlow Essex, U.K. In 1992, he was promoted to Professor of microelectronic engineering, and is currently Director of the Northern Ireland Semiconductor Research Centre. His research area is in silicon-device design and related technology, and he has lead projects on polysilicon and submicron gate MOST's, charge-coupled devices (CCD's), silicided shallow junctions, rapid thermal CVD, gate turn-off thyristors (GTO's) and static induction thyristors. His current main projects include SiGe epitaxial growth, direct silicon wafer bonding, thin-film transistors on glass, and high-density interconnects. He has co-authored over 140 publications in these areas.